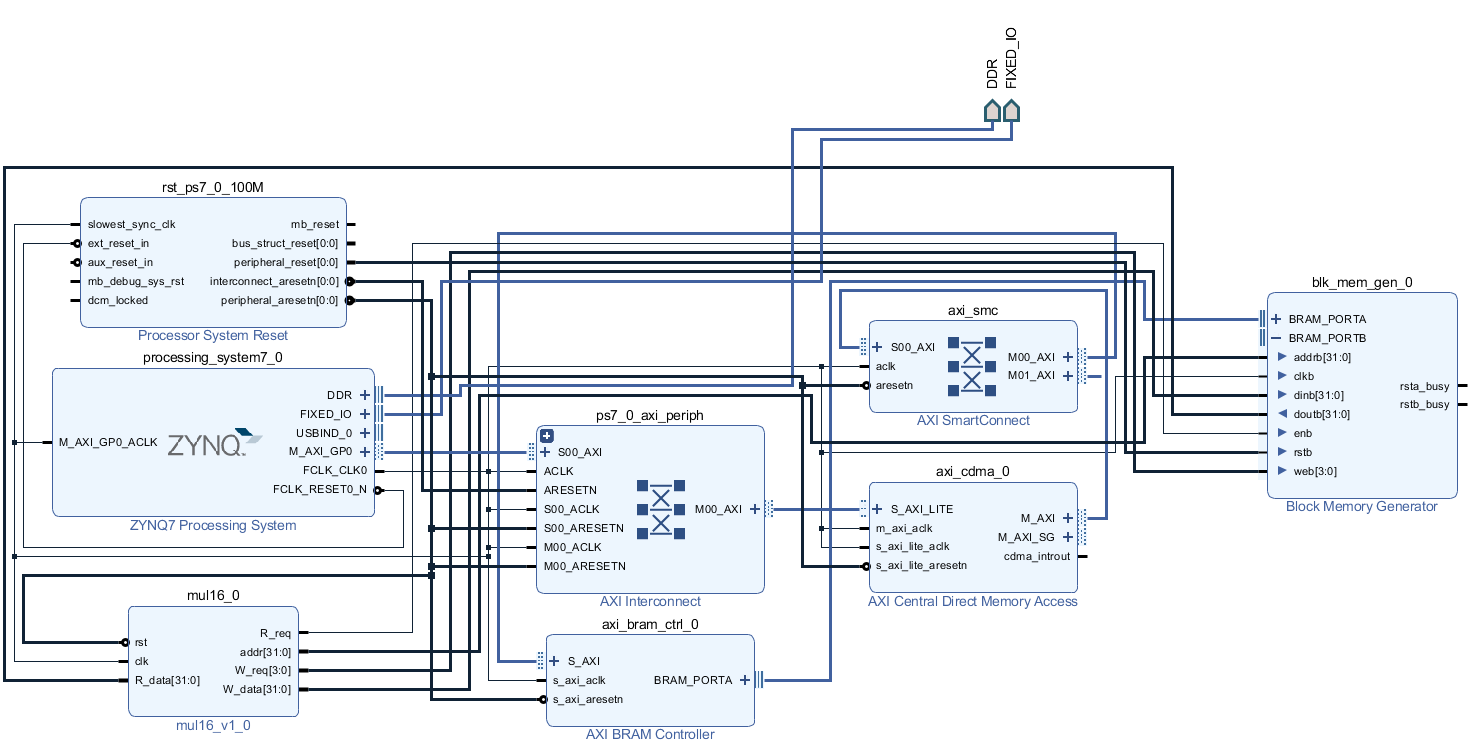
HOMEWORK 4

Student ID: P76087099 Name: NGUYEN VU LE MINH

**Block design Screenshot:**

(Please attach a screenshot and describe the block design function.)

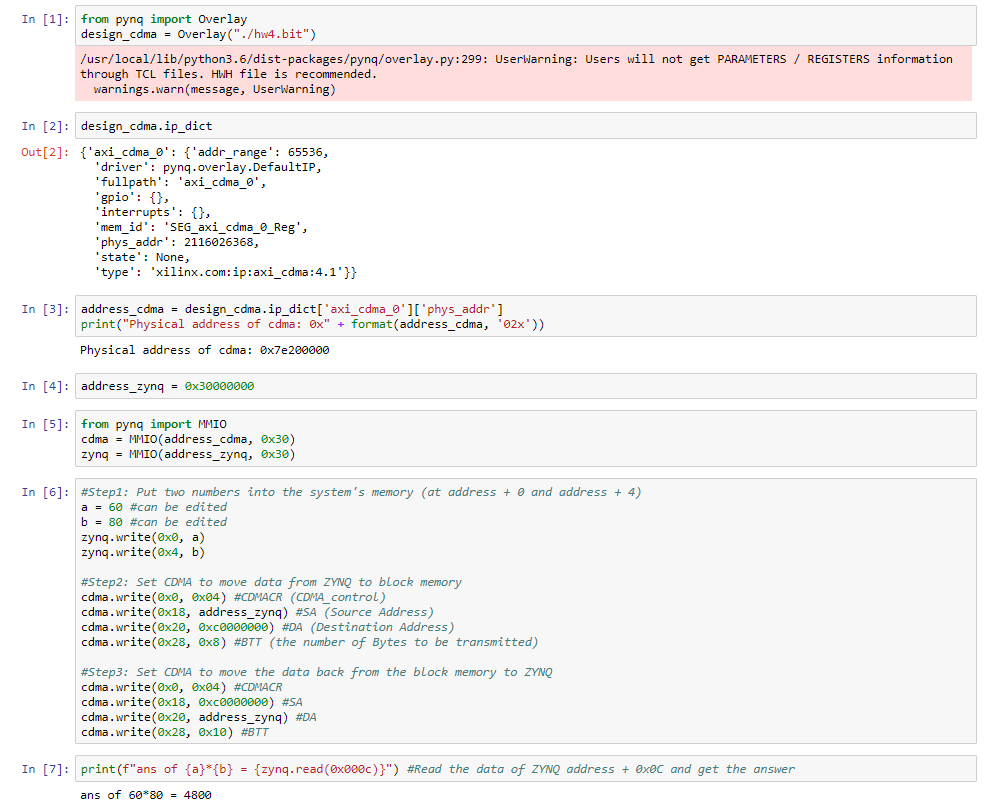


There are 7 main blocks that are: ZYNQ7 Processing system, AXI BRAM Controller, AXI Central Direct Memory Access, Mul16\_v1\_0 , Processor system reset, Block Memory Generator and AXI interconnect.

* ZYNQ7 Processing system: consists of an system-on-chip (SoC) style integrated processing system (PS) and a Programmable Logic (PL) unit, providing an extensible and flexible SoC solution on a single die.
* AXI BRAM Controller: The AXI bram controller is an IP provided by Xilinx vivado. It mainly converts the block memory read and write signals into AXI format, allowing block memory to communicate with AXI BUS.
* AXI Central Direct Memory Access (CDMA): is an IP provided by Xilinx vivado that can move data between two memory addresses. Like a normal DMA, CDMA has both Master and Slave pins on the system.
* Mul16\_v1\_0: This block can be put into hardware integrated circuit by IP, and the corresponding software design is completed to verify the functionality of the system. This block will perform the multiplication, and reads the data with the block memory address of 0x00 and 0x04. After multiplying, it is placed in 0x0C, so reading 0x0C of block memory can get the multiplication result.
* Processor system reset: allows the customer to tailor the design to suit their application by setting certain parameters to enable/disable features.
* Block Memory Generator: is an IP provided by Xilinx vivado, which can generate Block memory. It is similar to the general sram. It can adjust various parameters, such as memory size, single port or dual port, etc. It is a bit like memory compiler, block memory.
* AXI interconnect: connecting one or more AXI memory-mapped Master devices to one or more memory-mapped Slave devices.

**Jupyter python code:**

(Please describe the function and execution flow of the jupyter python code.)



* In the input [1], we read the hw4.bit which contains all information of hardware and it is exported by Vivado.
* In the input [2], we use a command that is “design\_cdma.ip\_dict” which is used to determine information in dictionary IPs. The important information is included that the IP driver, physical address, version.
* In the input [3], the address\_cdma value is a dictionary mapping the physical address. The operation address of Cdma is 0x7e200000.
* In the input [4], the create an address for kit Zynq.
* In the input [5], the library MMIO is used to map value of variables with IO address of hardware. Result will be showed depend on the calculation of Mul16\_v1\_0.
* In the input[6], The inputs (a and b) is entered will be transferred to Zynq to calculate by CDMA was be configured address. After that, the software will be read result by address “0x000c”. And the result is printed at the input[7]

**Lesson learn**

(Please write down the experience of completing this assignment, what you learned, and the points of difficulty.)

When I finished this homework, I learned many knowledge about design hardware by Vivado. Beside that, I can create a multiplication system which transfers data from CDMA to Block memory. After the hardware is calculated, the data is moved back to ZYNQ by CDMA.

About Jupyter, I learned how to set address for cdma and zynq. From that. I can transfer value to block memory to calculate and receive the result to display.